Synopsys Timing Constraints And Optimization User Guide

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Synopsys® Timing Constraints and Optimization User Guide Version D-2010.03, March 2010

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by Synplify Pro for FPGA synthesis: Timing Constraints User's Guide If necessary, change the design logic or adjust your timing constraints as described in Assigning Pins, Logic Options, and t SU, t CO & t PD Timing Constraints, then re-optimize the design.

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Timing Constraints _ optimization User guide.pdf - Synopsys...

The Galaxy Constraint Analyzer is an intuitive tool that enables designers to quickly assess the correctness and consistency of timing constraints. Correctness and consistency lead to more efficient runtimes in Synopsys' Design Compiler® synthesis and IC Compiler physical implementation tools.

Synopsys Introduces Galaxy Constraint Analyzer to Improve ...

• Creating the timing constraints using the SCOPE (Synthesis Constraints Optimization Environment) GUI available in Synplify Pro software. Constraints created using SCOPE are saved to a constraints file using the FDC format. Supported Synplify Pro Timing Constraints The following

timing constraints are supported by Synplify Pro for FPGA synthesis:

Timing Constraints User's Guide

Static timing analysis checks the timing across all paths in the design (regardless of whether these paths can actually be used in practice) and finds the longest path. For more information about static timing analysis, consult Chapter 1 of the Synopsys Timing Constraints and Optimization User Guide.

ECE 5745 Tutorial 5: Synopsys/Cadence ASIC Tools

Synopsys' PrimeTime static timing analysis tool provides a single, golden, trusted signoff solution for timing, signal integrity, power and variation-aware analysis. It delivers HSPICE® accurate signoff analysis that helps pinpoint problems prior to chip tapeout thereby reducing risk, ensuring design integrity, and lowering the cost of design.

Gold Standard in Static Timing Analysis - Synopsys

Galaxy Constraint Analyzer provides an extensive set of rule checks designed to maximize the efficiency of the Synopsys Galaxy Design Platform. Galaxy Constraint Analyzer uses technology based on the Synopsys golden PrimeTime timing engine to ensure correct interpretation and propagation of constraints.

Boosting Designer Productivity by Using Look ... - Synopsys

constraints: rules from library vendor for proper functioning of the fabricated circuit Must not be violated Common constraints: transition time, fanout load, capacitance Design optimization . constraints: user-specified timing and area optimization goals DC tries to optimize these without violating design rules Common constraints: timing and area

Automated Synthesis from HDL models

If necessary, change the design logic or adjust your timing constraints as described in Assigning Pins, Logic Options, and t SU, t CO & t PD Timing Constraints, then re-optimize the design. Continue with the steps necessary to process your design, as described in Synthesizing & Optimizing VHDL or Verilog HDL Files with FPGA Express Software.

Using Synopsys FPGA Express & MAX+PLUS II Software

and timing constraints posted into the design, and would not degrade the timing QOR of the design post leakage optimization flow. Besides, fix_eco_leakage works well with the Primetime

(PDF) Optimum Leakage Recovery using Synopsys Primetime ...

In this tutorial you will use Synopsys Design Compiler to elaborate RTL, set optimization constraints, synthesize to gates, and prepare various area and timing reports. You will also learn how to read the various DC text reports and how to use the graphical Synopsys Design Vision tool to visualize the synthesized design.

RTL-to-Gates Synthesis using Synopsys Design Compiler

DC FPGA's Adaptive Optimization technology contains new, advanced optimizations that automatically activate the best core synthesis algorithms based on multiple parameters, including design size, circuit topology and timing constraints, then dynamically control and reorder how the algorithms are applied.

Synopsys Delivers New FPGA Synthesis Solution to Solve the ...

Timing Constraint Model. In SYNOPSYS, there are four types of timing paths (seeFigure 1): Figure 1. Timing Path Types. Primary input to register. These paths are usually constrained by specifying theclock for register and setting an input delay relative to a clock on theinput port. Register to

register.

SYNOPSYS1
R&D Engineer at Synopsys Inc ... with reduced area and power given timing constraints. ... Transistor-level static timing analyzer and timing / power optimization by incrementally updating timing ...

Seung-Il Kang - R&D Engineer - Synopsys Inc | LinkedIn
*Performed synthesis ,place and route of large blocks using Synopsys tools (DC/ICC). *Extensive use of timing closer techniques like incremental optimization, path groups, placement blockages, logic bounds, keepout margin and cell density control option. Constraint analysis and review for cleaner SDC and improving the... Block owner:

Jan Balakayev - Senior Physical Design Engineer - Cisco ...
The solutions were used by leading foundry and fabless customers to route billion-scale devices under extremely complex optimization constraints (e.g. area, routing congestion, stringent timing ...

Jianfeng Luo - Technical Director / Principal R&D Engineer ...
Timing budgeting distributes positive and negative slack between blocks and then generates timing constraints in the Synopsys Design Constraints (SDC) format for block-level implementation. To generate a pre-budgeting timing analysis report file, use the check_fp_timing_environment command. To run the timing budgeter, use the allocate_fp_budgets command. Immediately after budgeting a design, you can use the check_fp_budget_result command to perform post-budget analysis. [16]